1 PRODUCT OVERVIEW

The S3C7044/C7048 single-chip CMOS microcontroller has been designed for very high-performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

The S3P7048 is the microcontroller which has 8K-bytes one-time-programmable ROM and the functions are same to S3C7044/C7048.

With two 8-bit timer/counters, an 8-bit serial I/O interface, and eight software n-channel open-drain I/O pins, the S3C7044/C7048 offers an excellent design solution for a wide variety of general-purpose applications.

Up to 36 pins of the 42-pin SDIP or 44-pin QFP package can be dedicated to I/O. Seven vectored interrupts provide fast response to internal and external events.

In addition, the S3C7044/C7048's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

FEATURES SUMMARY

Memory

- 512 × 4-bit RAM
- 4096 × 8-bit ROM: S3C7044
- 8192 × 8-bit ROM: S3C7048

36 I/O Pins

- Input only: 4 pins
- I/O: 24 pins
- N-channel open-drain I/O: 8 pins

Memory-Mapped I/O Structure

- Data memory bank 15

8-Bit Basic Timer

- 4 interval timer functions

Two 8-Bit Timer/Counters

- Programmable interval timer
- External event counter function
- Timer/counters clock outputs to TCLO0 and TCLO1 pins

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 4.19 MHz
- 4 frequency outputs to the BUZ pin

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Interrupts

- 3 external interrupt vectors
- 4 internal interrupt vectors
- 2 quasi-interrupts

Power-Down Modes

- Idle: Only CPU clock stops
- Stop: System clock stops

Oscillation Sources

- Crystal or Ceramic for system clock
- Oscillation frequency : 0.4 – 6.0MHz
- CPU clock divider circuit (by 4. 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 µs at 4.19 MHz
- 0.67, 1.33, 10.7 µs at 6.0 MHz

Operating Temperature

- - 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V (Main)
- 2.0 V to 5.5 V (OTP)

Package Types

- 42-pin SDIP, 44-pin QFP

FUNCTION OVERVIEW

SAM47 CPU

All S3C7-series microcontrollers have the advanced SAM47 CPU core. The SAM47 CPU can directly address up to 32K-byte of program memory. The arithmetic logic unit(ALU) performs 4-bit addition, subtraction, logical, and shift-and-rotate operations in one instruction cycle and most 8-bit arithmetic and logical operation in two cycles.

CPU REGISTERS

program counter

A 12-bit program counter (PC) stores addresses for instruction fetches during program execution. Usually, the PC is incremented by the number of bytes of the fetched instruction. The one instruction fetch that does not increment the PC is the 1-byte REF instruction which references instruction stored in a look-up table in the ROM. Whenever a reset operation or an interrupt occurs, bits PC12 though PC0 are set to the vector address.

Stack pointer

An 8-bit stack pointer (SP) stores addresses for stack operation. The stack area is located in general-purpose data memory bank 0. The SP is 8-bit read/writeable and SP bit 0 must always be logic zero.

During an interrupt or a subroutine call, the PC value and the PSW are written to the stack area. When the service routine has completed, the values referenced by the stack pointer are restored. Then, the next instruction is executed.

The stack pointer can access the stack despite data memory access enable flag status. Since the reset value of the stack pointer is not defined in firmware, you use program code to initialize the stack pointer to 00H. This sets the first register of the stack area to data memory location 0FFH.

PROGRAM MEMORY

In its standard configuration, the 4096 x 8-bit (S3C7404), 8192 x 8-bit (S3C7408) ROM is divided into four areas:

— 16-byte area for vector addresses
— 96-byte instruction reference area
— 16-byte general-purpose area (0010 – 001FH)
— 3968-byte area for general-purpose program memory (S3C7404)
— 8064-byte area for general-purpose program memory (S3C7408)

The vector address area is used mostly during reset operation and interrupts. These 16 bytes can alternately be used as general-purpose ROM.

The REF instruction references 2x1-byte or 2-byte instruction stored in reference area location 0020H – 007FH. REF can also reference three-byte instruction such as JP or CALL. So that a REF instruction can reference these instruction, however, the JP or CALL must be shortened to a 2-byte format. To do this, JP or CALL is written to the reference area with the format TJP or TCALL instead of the normal instruction name. Unused location in the REF instruction look-up area can be allocated to general-purpose use.

DATA MEMORY

Overview

The 512 x 4bit data memory has five areas:

- 32 x 4-bit working register area
- 224 x 4-bit general-purpose area in bank 0 which is also used as the stack area
- 256 x 4-bit general-purpose area in bank 1
- 128 x 4-bit area in bank 15 for memory-mapped I/O addresses

The data memory area is also organized as three memory banks — bank0, bank1, and bank15. You use the select memory bank instruction (SMB) to select one of the banks as working data memory.

Data stored in RAM location are 1-, 4-, and 8-bit addressable. After a hardware reset, data memory initialization values must be defined by program code.

Data Memory addressing modes

The enable memory bank (EMB) flag controls the addressing mode for data memory banks 0, 1, or 15. When the EMB flag is logic zero, only location 00H–7FH of bank 0 and bank 15 can be accessed. When the EMB flag is set to logic one, all three data memory banks can be accessed based on the current SMB value.

Working registers

The RAM's working register area in data memory bank 0 is also divided into four register banks. Each register bank has eight 4-bit registers. Paired 4-bit registers are 8-bit addressable.

Register A can be used as a 4-bit accumulator and double register EA as an 8-bit extended accumulator; double registers WX, WL, and HL are used as address pointers for indirect addressing.

To limit the possibility of data corruption due to incorrect register addressing, it is advisable to use bank 0 for main programs and banks 1, 2, and 3 for interrupt service routines.

Bit sequential carrier

The bit sequential carrier (BSC) mapped in data memory bank 15 is a 16-bit general register that you can manipulate using 1-, 4-, and 8-bit RAM control instructions.

Using the BSC register, addresses and bit location can be specified sequentially using 1-bit indirect addressing instructions. In this way, a program can generate 16-bit data output by moving the bit location sequentially, incrementing or decrementing the value of the L register. You can also use direct addressing to manipulate data in the BSC.

CONTROL REGISTERS

Program Status Word

The 8-bit program status word (PSW) controls ALU operation and instruction execution sequencing. It is also used to restore a program's execution environment when an interrupt has been serviced. Program instructions can always address the PSW regardless of the current value of data memory access enable flags.

Before an interrupt is processed, the PSW is pushed onto the stack in data memory bank 0. When the routine is completed, PSW values are restored.

IS1	IS0	EMB	ERB
C	SC2	SC1	SC0

Interrupt status flags (IS1, IS0), the enable memory bank and enable register bank flags (EMB, ERB), and the carry flag (C) are 1- and 4-bit read/write or 8-bit read-only addressable. Skip condition flags (SC0–SC2) can be addressed using 8-bit read instructions only.

Select Bank (SB) Register

Two 4-bit location called the SB register store address values used to access specific memory and register banks: the select memory bank register, SMB, and the select register bank register, SRB.

'SMB n' instructions select a data memory bank (0, 1, or 15) and store the upper four bits of the 12-bit data memory address in the SMB register. The 'SMB n' instruction is used to select register bank 0, 1, 2, or 3, and to store the address data in the SRB.

The instructions 'PUSH SB' and 'POP SB' move SMB and SRB values to and from the stack for interrupts and subroutines.

CLOCK CIRCUITS

System oscillation circuit generates the internal clock signals for the CPU and peripheral hardwares. The system clock can use a crystal, ceramic, or RC oscillation source, or an externally-generated clock signal. To drive S3C7044/C7048 using an external clock source, the external clock signal should be input to X_{in}, and its inverted signal to X_{out}.

A 4-bit power control register is used to enable or disable oscillation, and to select the CPU clock. The internal system clock signal (fx) can be divided internally to produce three CPU clock frequencies — fx/4, fx/8, or fx/64.

INTERRUPTS

Interrupt requests can be generated internally by on-chip processes (INTB, INTT0, INTT1, and INTS) or externally by peripheral devices (INT0, INT1, and INT4). There are two quasi-interrupts: INT2 and INTW.

INT2/KS0–KS7 detects rising/falling edges of incoming signals and INTW detects time intervals of 0.5 seconds of 3.91 milliseconds at 4.19MHz. The following components support interrupt processing:

- Interrupt enable flags
- Interrupt request flags
- Interrupt priority registers
- Power-down termination circuit

POWER-DOWN

To reduce power consumption, there are two power-down modes: idle and stop. The IDLE instruction initiates idle mode and the STOP instruction initiates stop mode.

In idle mode, only the CPU clock stops while peripherals and the oscillation source continue to operate normally. Stop mode effects only the system clock. In stop mode system clock oscillation stops completely, halting all operations except for a few basic peripheral functions. RESET or an interrupt (with the exception of INT0) can be used to terminate either idle or stop mode.

RESET

When a RESET signal occurs during normal operation or during power-down mode, the CPU enters idle mode when the reset operation is initiated. When the standard oscillation stabilization interval (31.3 ms at 4.19 MHz) has elapsed, normal CPU operation resumes.

I/O PORTS

The S3C7044/C7048 has 9 I/O ports. Pin addresses for all I/O ports are mapped to locations FF0H–FFCH in bank 15 of the RAM.

There are 4 input pins, 24 configurable I/O pins, and 8 software n-channel open-drain I/O pins, for a total of 36 I/O pins. The contents of I/O port pin latches can be read, written, or tested at the corresponding address using bit manipulation instructions.

TIMERS AND TIMER/COUNTERS

The timer function has four main components: an 8-bit basic interval timer, two 8-bit timer/counters, and a watch timer. The 8-bit basic timer generates interrupt requests at precise intervals, based on the selected CPU clock frequency.

The programmable 8-bit timer/counters are used for external event counting, generation of arbitrary clock frequencies for output, and dividing external clock signals. The 8-bit timer/counter 0 generates a clock signal (SCK) for the serial I/O interface.

The watch timer has an 8-bit watch timer mode register, a clock selector, and a frequency divider circuit. Its functions include real-time and watch-time measurement, and frequency outputs for buzzer sound.

SERIAL I/O INTERFACE

The serial I/O interface supports the transmission or reception of 8-bit serial data with an external device. The serial interface has the following functional components:

- 8-bit mode register
- Clock selector circuit
- 8-bit buffer register
- 3-bit serial clock counter

The serial I/O circuit can be set either to transmit-and-receive or to receive-only mode. MSB-first or LSB-first transmission is also selectable. The serial interface operates with an internal or an external clock source, or using the clock signal generated by the 8-bit timer/counter 0. To modify transmission frequency, the appropriate bits in the serial I/O mode register (SMOD) must be manipulated.

BLOCK DIAGRAM

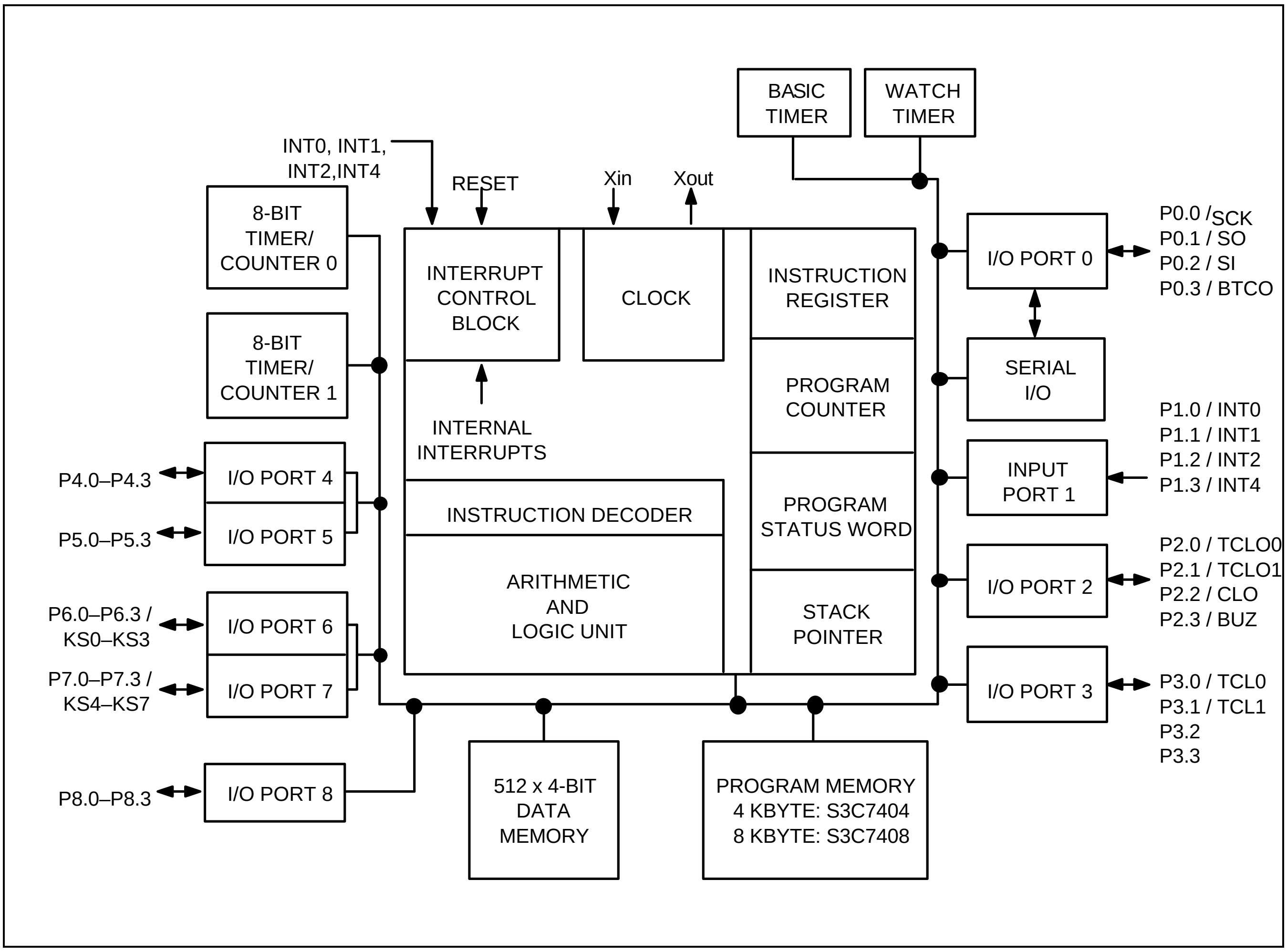


Figure 1-1. S3C7044/C7048/P0408 Block Diagram

PIN ASSIGNMENTS

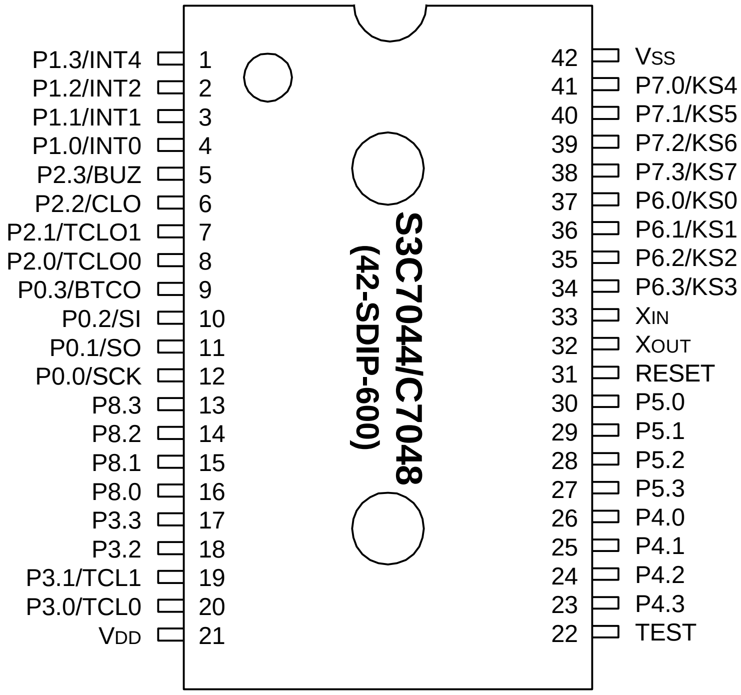


Figure 1-2. S3C7044/C7048 Pin Assignment Diagrams (42-SDIP Pakage)

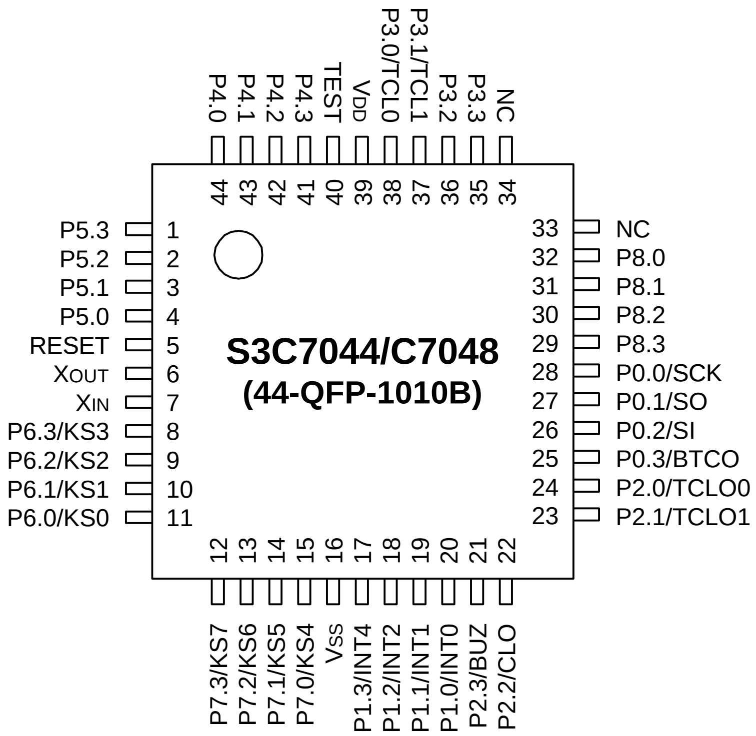


Figure 1-3. S3C7044/C7048 Pin Assignment Diagrams (44-QFP Pakage)

PIN DESCRIPTIONS

Table 1-1. S3C7044/C7048/P0408 Pin Description

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	12 (28) 11 (27) 10 (26) 9 (25)	SCK SO SI BTCO
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 3-bit pull-up resistors are assignable by software to pins P1.0, P1.1, and P1.2.	4 (20) 3 (19) 2 (18) 1 (17)	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0.	8 (24) 7 (23) 6 (22) 5 (21)	TCLO0 TCLO1 CLO BUZ
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0.	20 (38) 19 (37) 18 (36) 17 (35)	TCL0 TCL1
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. N-channel open-drain output up to 9 volts. 1-bit and 4-bit read/write and test is possible. Ports 4 and 5 can be paired to support 8-bit data transfer. 8-bit unit pull-up resistors are assignable by mask option.	26–23 (44–41) 30–27 (4–1)	–
P6.0–P6.3 P7.0–P7.3	I/O	4-bit I/O ports. 1-bit or 4-bit read/write and test is possible. Port 6 pins are individually software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins (port 6 only). Ports 6 and 7 can be paired to enable 8-bit data transfer.	37–34 (11–8) 41–38 (15–12)	KS0–KS3 KS4–KS7
P8.0–P8.3	I/O	4-bit I/O ports. 1-bit and 4-bit read/write and test is possible. Pins are individually software configurable as input or output. 4-bit pull-down resistors are software assignable; pull-down resistors are automatically disabled for output pins.	16–13 (32–29)	–

NOTE: Parentheses indicate pin number for 44 QFP package.

Table 1-1. S3C7044/C7048 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
SCK	I/O	Serial I/O interface clock signal	12 (28)	P0.0
SO	I/O	Serial data output	11 (27)	P0.1
SI	I/O	Serial data input	10 (26)	P0.2
BTCO	I/O	Basic timer clock output (2 Hz, 16 Hz, 64 Hz, or 256 Hz at 4.19 MHz)	9 (25)	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. INT0 is synchronized to system clock.	4, 3 (20, 19)	P1.0, P1.1
INT2	I	Quasi-interrupt with detection of rising edges	2 (18)	P1.2
INT4	I	External interrupt with detection of rising and falling edges.	1 (17)	P1.3
TCLO0	I/O	Timer/counter 0 clock output	8 (24)	P2.0
TCLO1	I/O	Timer/counter 1 clock output	7 (23)	P2.1
CLO	I/O	Clock output	6 (22)	P2.2
BUZ	I/O	2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at 4.19 MHz for buzzer sound	5 (21)	P2.3
TCL0	I/O	External clock input for timer/counter 0	20 (38)	P3.0
TCL1	I/O	External clock input for timer/counter 1	19 (37)	P3.1
KS0–KS3 KS4–KS7	I/O	Quasi-interrupt inputs with falling edge detection	37–34 (11–8) 41–38 (15–12)	P6.0–P6.3 P7.0–P7.3
V_{DD}	–	Power supply	21 (39)	–
V_{SS}	–	Ground	42 (16)	–
RESET	I	Reset signal	31 (5)	–
X_{in}, X_{out}	–	Crystal, ceramic, or RC oscillator signal for system clock (For external clock input, use X_{in} and input X_{in}'s reverse phase to X_{out})	33, 32 (7, 6)	–
TEST	–	Test signal input (must be connected to V_{SS})	22 (40)	–
NC	–	No connection (must be connected to V_{SS})	(33, 34)	–

NOTE: Parentheses indicate pin number for 44 QFP package.

Table 1-2. Overview of S3C7044/C7048 Pin Data

Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
P0.0–P0.3	SCK, SO, SI, BTCO	I/O	Input	D-1
P1.0–P1.2	INT0, INT1, INT2	I	Input	A-3
P1.3	INT4	I	Input	B-4
P2.0–P2.3	TCLO0, TCLO1, CLO, BUZ	I/O	Input	D
P3.0–P3.1	TCL0, TCL1	I/O	Input	D-1
P3.2–P3.3	–	I/O	Input	D
P4.0–P4.3 P5.0–P5.3	–	I/O	(NOTE)	E-2
P6.0–P6.3 P7.0–P7.3	KS0–KS3 KS4–KS7	I/O	Input	D-1
P8.0–P8.3	–	I/O	Input	D-2
X_{in}, X_{out}	–	–	–	–
RESET	–	I	–	B
TEST	–	I	–	–
NC	–	–	–	–
V_{DD}, V_{SS}	–	–	–	–

NOTE: When pull-up resistors are provided, port 4 and port 5 pins are reset to high level; with no pull-ups, they are reset to high impedance.

PIN CIRCUIT DIAGRAMS

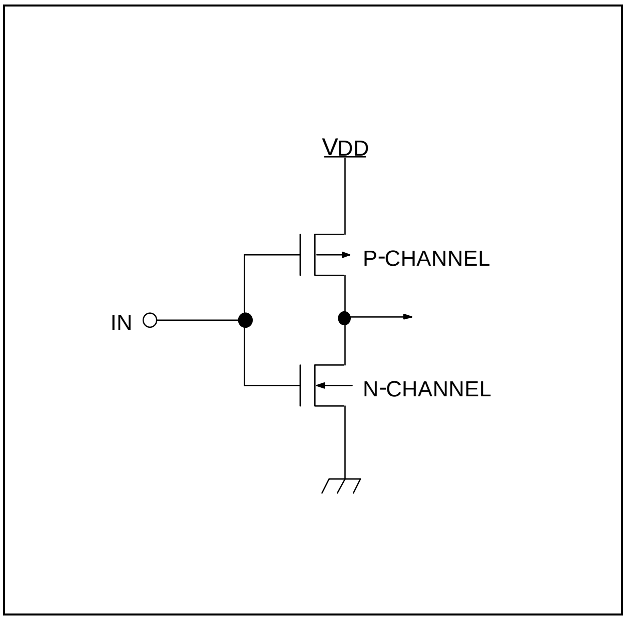


Figure 1-4. Pin Circuit Type A

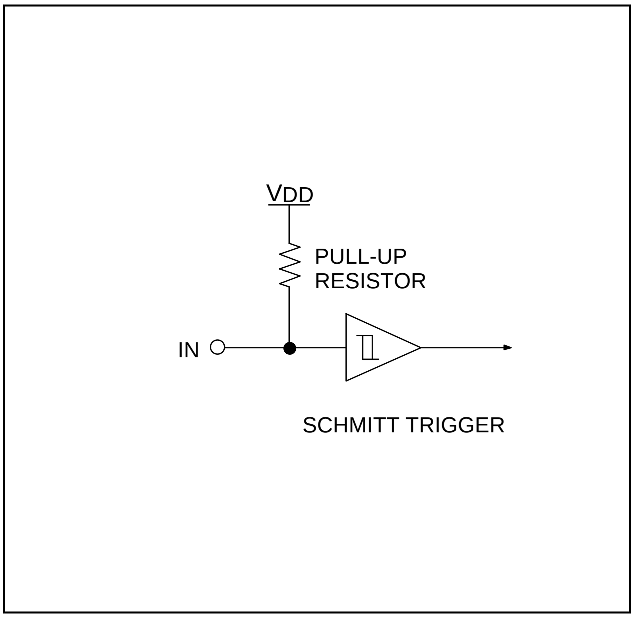


Figure 1-6. Pin Circuit Type B

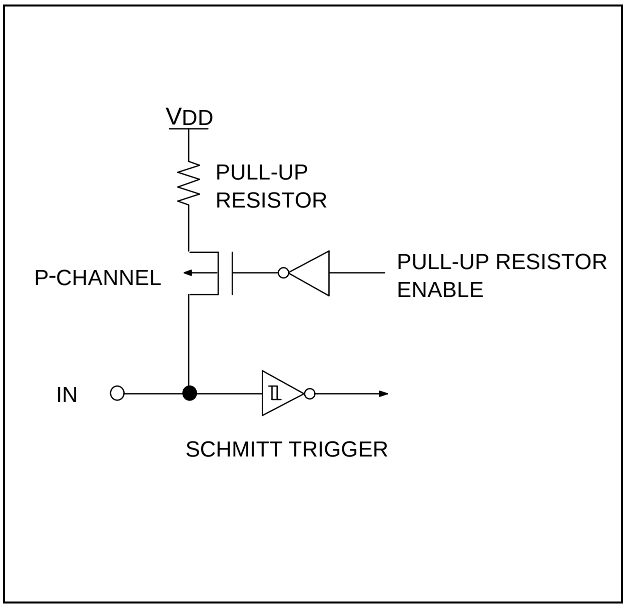


Figure 1-5. Pin Circuit Type A-3

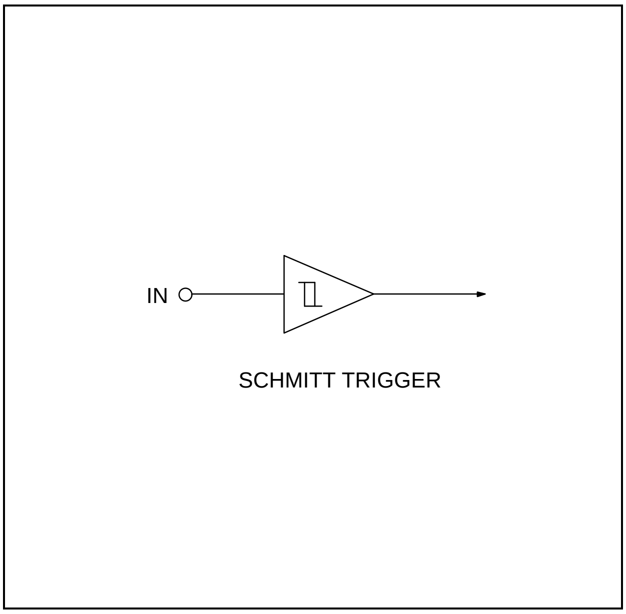


Figure 1-7. Pin Circuit Type B-4

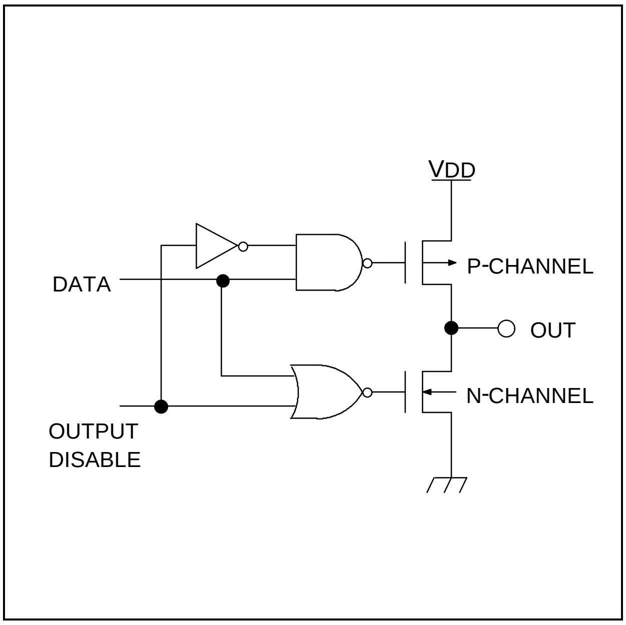


Figure 1-8. Pin Circuit Type C

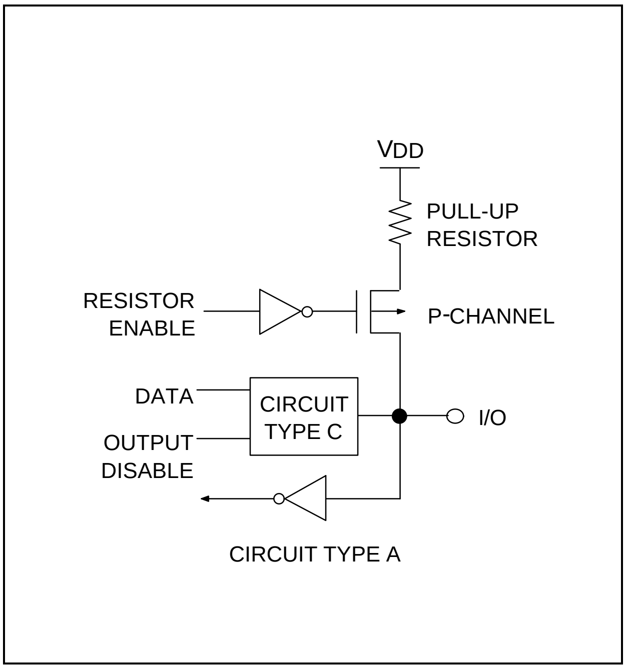


Figure 1-9. Pin Circuit Type D

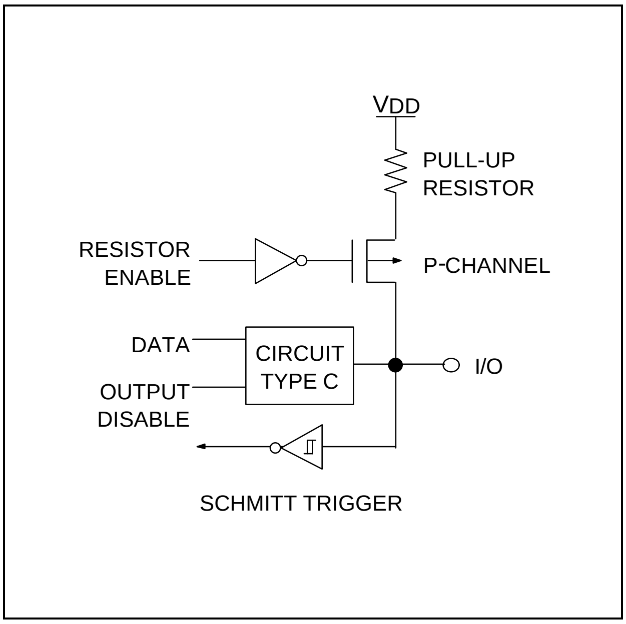


Figure 1-10. Pin Circuit Type D-1

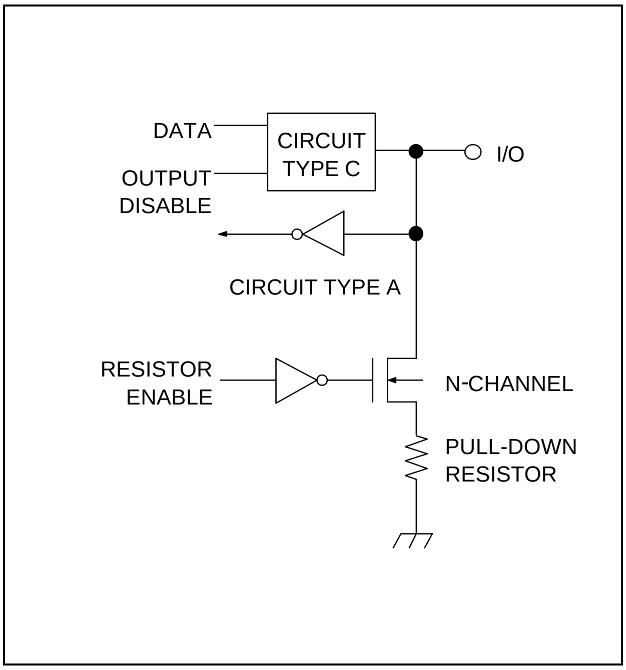


Figure 1-11. Pin Circuit Type D-2

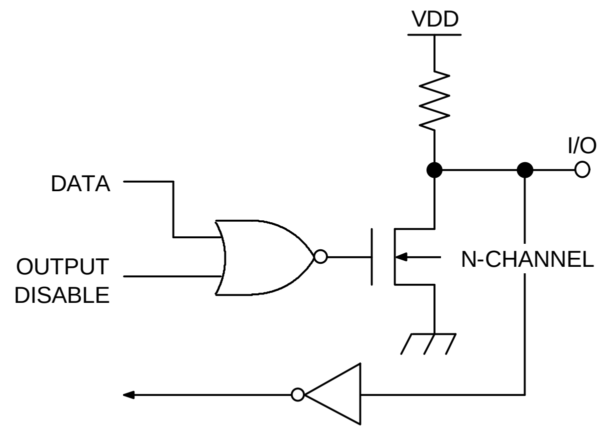


Figure 1-12. Pin Circuit Type E-2

13 ELECTRICAL DATA

In this section, information on S3C7044/C7048 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— System clock oscillator characteristics
— I/O capacitance
— A.C. electrical characteristics
— Operating voltage range

Miscellaneous Timing Waveforms

— A.C timing measurement point
— Clock timing measurement at X_{IN} and X_{OUT}
— TCL timing
— Input timing for RESET
— Input timing for external interrupts
— Serial data transfer timing

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Table 13-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_{I1}	All I/O ports except 4 and 5	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	– 15	mA
		All I/O ports active	– 30	
Output Current Low	I_{OL}	One I/O port active	+ 30 (Peak value)	mA
			+ 15 (note)	
		All I/O ports, total	+ 100 (Peak value)	
			+ 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

NOTE: The values for output current low (I_{OL}) are calculated as peak value $\times \sqrt{Duty}$.

SAMSUNG ELECTRONICS

Table 13-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except those specified below for V_{IH2} – V_{IH4}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 3, 6, 7, and RESET	0.8 V_{DD}			
	V_{IH3}	Ports 4 and 5 with pull-up resistors assigned	0.7 V_{DD}			
		Ports 4 and 5 are open-drain				
	V_{IH4}	X_{IN} and X_{OUT}	V_{DD} – 0.1			
Input Low Voltage	V_{IL1}	All input pins except those specified below for V_{IL2}–V_{IL3}	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 3, 6, 7, and RESET			0.2 V_{DD}	
	V_{IL3}	X_{in} and X_{out}			0.1	
Output High Voltage	V_{OH}	I_{OH} = – 1 mA Ports except 1, 4, and 5	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA, Ports 4, 5 only	–	–	2	V
		V_{DD} = 1.8 to 5.5 V I_{OL} = 1.6mA			0.4	
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V I_{OL}= 4 mA All output ports except ports 4,5			2	
		V_{DD} = 1.8 to 5.5 V I_{OL} = 1.6mA			0.4	
Input High Leakage Current	I_{LIH1}	V_I = V_{DD} All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	V_I = V_{DD} X_{IN} and X_{OUT}			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V All input pins except below and RESET	–	–	– 3	µA
	I_{LIL2}	V_I = 0 V X_{IN} and X_{OUT} only			– 20	

Table 13-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

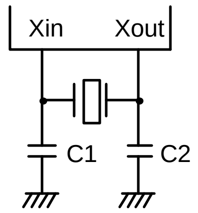
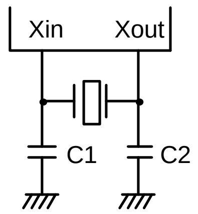
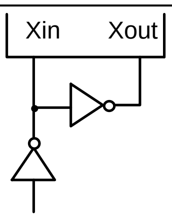
Parameter	Symbol	Conditions		Min	Typ	Max	Units
Output High Leakage Current	I_{LOH}	$V_O = V_{DD}$, All output pins		–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V, All output pins		–	–	– 3	µA
Pull-Up Resistor	R_{L1}	V_I = 0 V; V_{DD} = 5 V Ports 0, 1 (not P1.3), 2, 3, 6, 7		25	47	100	kΩ
		V_{DD} = 3 V		50	95	200	
	R_{L2}	$V_O = V_{DD}$ – 2V; V_{DD} = 5V Ports 4 and 5 only		15	47	70	
		V_{DD} = 3 V		10	45	60	
	R_{L3}	V_{DD} = 5 V; V_I = 0V; RESET		100	220	400	
		V_{DD} = 3 V		200	450	800	
Pull-Down Resistor	R_{L4}	V_{DD} = 5 V; $V_I = V_{DD}$; Port 8		25	47	100	kΩ
		V_{DD} = 3 V		50	95	200	
Supply Current (1)	I_{DD1}	Run mode; V_{DD} = 5 V ± 10%	6.0 MHz	–	3.9	8.0	mA
		Crystal oscillator; C1 = C2 = 22 pF	4.19 MHz		2.9	5.5	
		V_{DD} = 3 V ± 10%	6.0 MHz		1.8	4.0	
			4.19 MHz		1.3	3.0	
	I_{DD2}	Run mode; V_{DD} = 5 V ± 10%	6.0 MHz	–	1.3	2.5	mA
		crystal oscillator, C1 = C2 = 22 pF	4.19 MHz		1.2	1.8	
		V_{DD} = 3 V ± 10%	6.0 MHz		0.5	1.5	
			4.19 MHz		0.44	1.0	
	I_{DD3}	Stop mode; V_{DD} = 5 V ± 10%		–	0.2	3	µA
		Stop mode; V_{DD} = 3 V ± 10%			0.1	2	

NOTES

1. D.C. electrical values for Supply Current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up resistors.
2. The supply current assumes a CPU clock of fx/4.

Table 13-3. Main System Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency [1]	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	4.2	
		Stabilization time [2]	V_{DD} = 3 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency [1]	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	4.2	
		Stabilization time [2]	V_{DD} = 3 V	–	–	10	ms
External Clock		X_{IN} input frequency [1]	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	4.2	
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns

NOTES

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 13-4. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 13-5. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	μs
		V_{DD} = 1.8 V to 5.5 V	0.95			
TCL0, TCL1 Input Frequency	f_{TI0}, f_{TI1}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5V			1	
TCL0, TCL1 Input High, Low Width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	μs
		V_{DD} = 1.8 V to 5.5 V	1.8			
SCK Cycle Time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V External SCK source	800	–	–	μs
		Internal SCK source	670			
		V_{DD} = 1.8 V to 5.5 V External SCK source	3200			
		Internal SCK source	3800			
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 2.7 V to 5.5 V External SCK source	335	–	–	μs
		Internal SCK source	t_{KCY}/ 2 – 50			
		V_{DD} = 1.8 V to 5.5 V External SCK source	1600			
		Internal SCK source	t_{KCY}/ 2 – 150			

Table 13-5. A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SI Setup Time to SCK High	t_{SIK}	V_{DD} = 2.7 V to 5.5 V External SCK source	100	–	–	ns
		Internal SCK source	150			
		V_{DD} = 1.8 V to 5.5 V External SCK source	150			
		Internal SCK source	500			
SI Hold Time to SCK High	t_{KSI}	V_{DD} = 2.7 V to 5.5 V External SCK source	400	–	–	ns
		Internal SCK source	400			
		V_{DD} = 1.8 V to 5.5 V External SCK source	600			
		Internal SCK source	500			
Output Delay for SCK to SO	t_{KSO} (1)	V_{DD} = 2.7 V to 5.5 V External SCK source	–	–	300	ns
		Internal SCK source			250	
		V_{DD} = 1.8 V to 5.5 V External SCK source			1000	
		Internal SCK source			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0	(2)	–	–	µs
		INT1, INT2, INT4, KS0 - KS7	10			
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTES
1. R(1Kohm) and C(100pF) are the load resistance and load capacitance of the SO output line.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128/fx as assigned by the IMOD0 register setting.

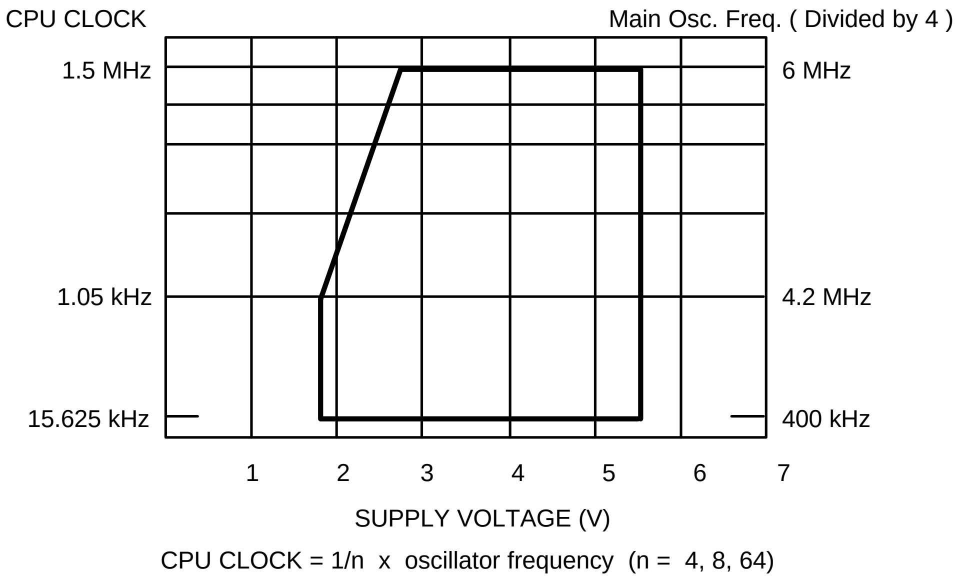


Figure 13-1. Standard Operating Voltage Range

Table 13-6. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.5	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.5 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17}/fx	–	ms
		Released by interrupt	–	(2)	–	ms

NOTES
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

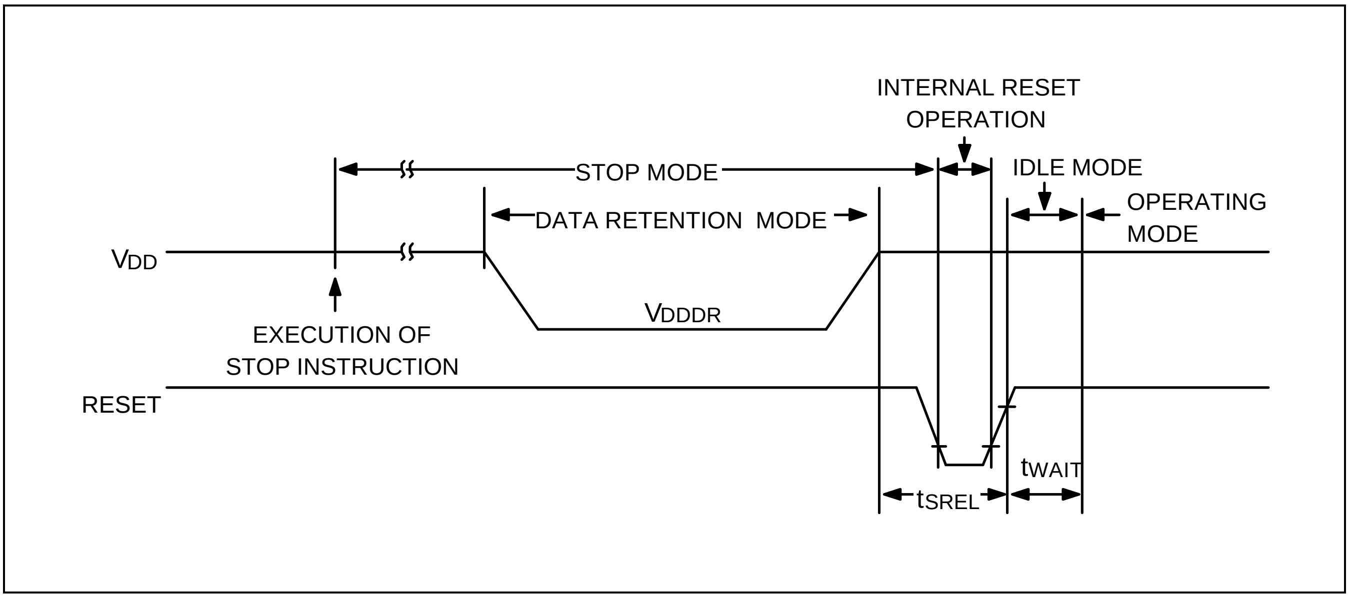


Figure 13-2. Stop Mode Release Timing When Initiated By RESET

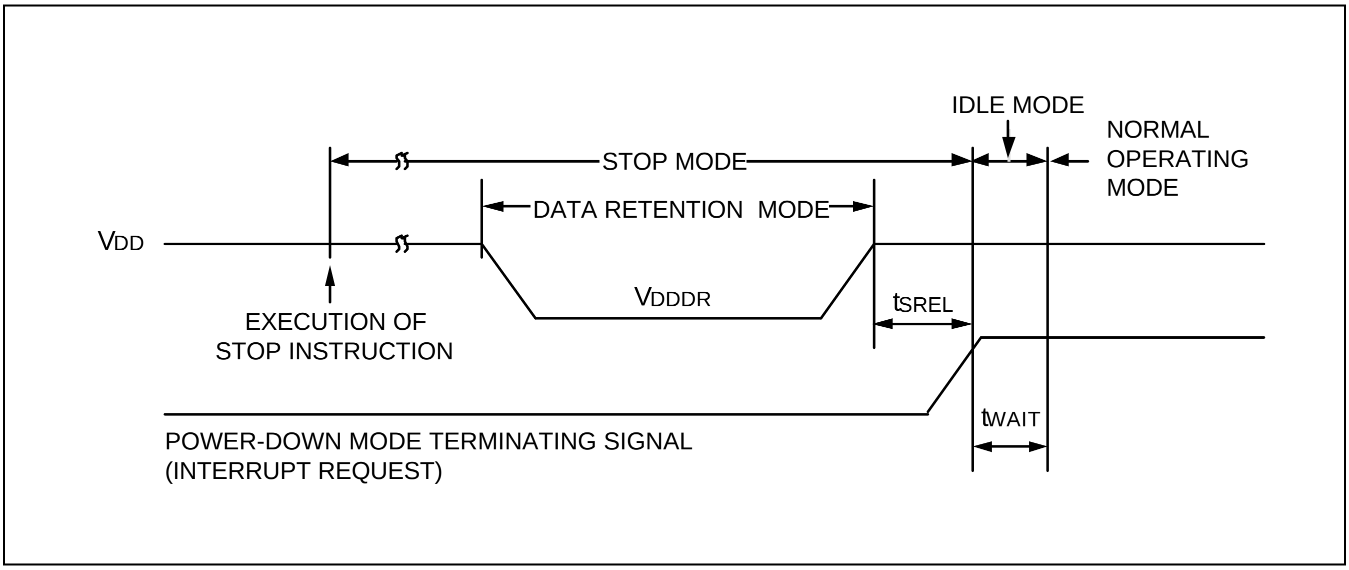


Figure 13-3. Stop Mode Release Timing When Initiated By Interrupt Request

Timing Waveforms (continued)

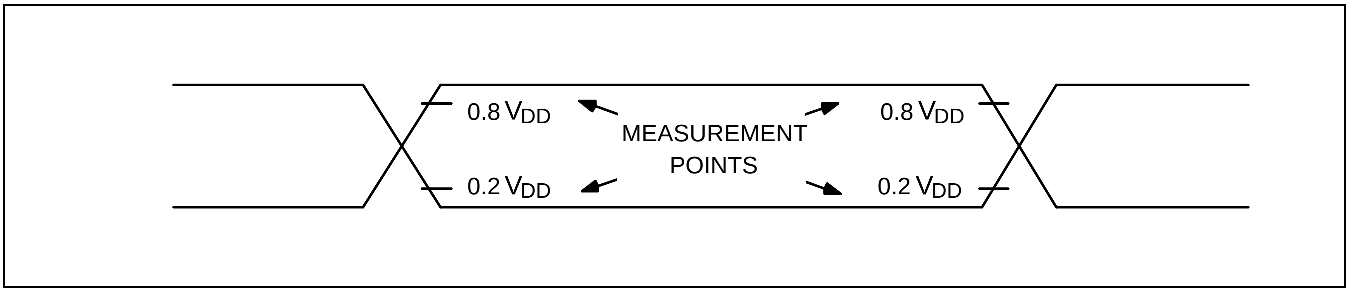


Figure 13-4. A.C. Timing Measurement Points (Except for X_{IN})

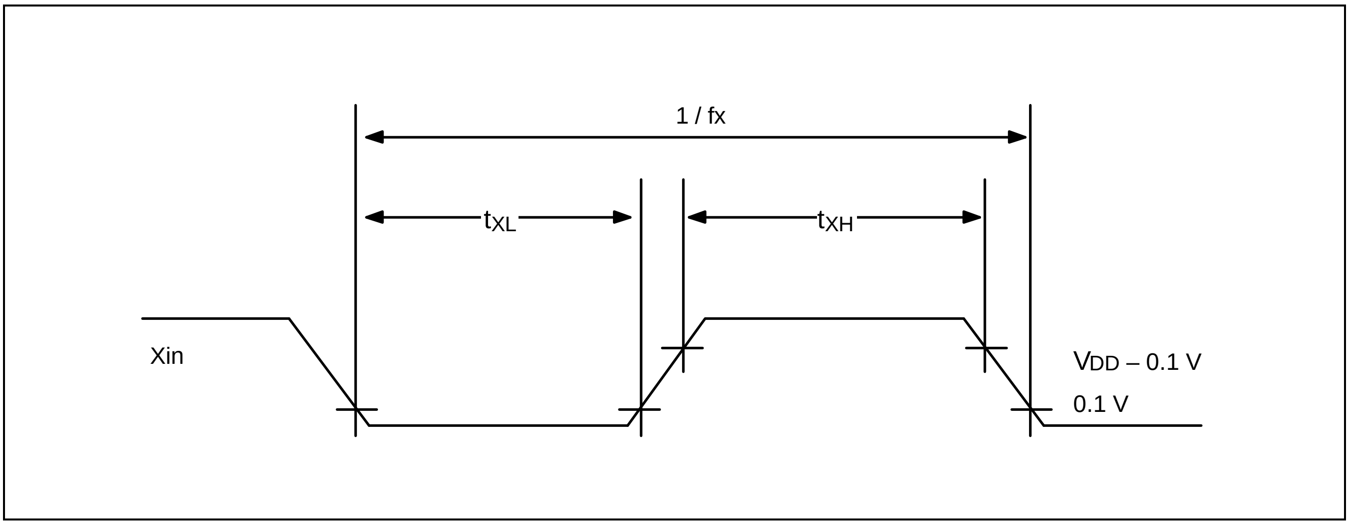


Figure 13-5. Clock Timing Measurement at X_{IN}

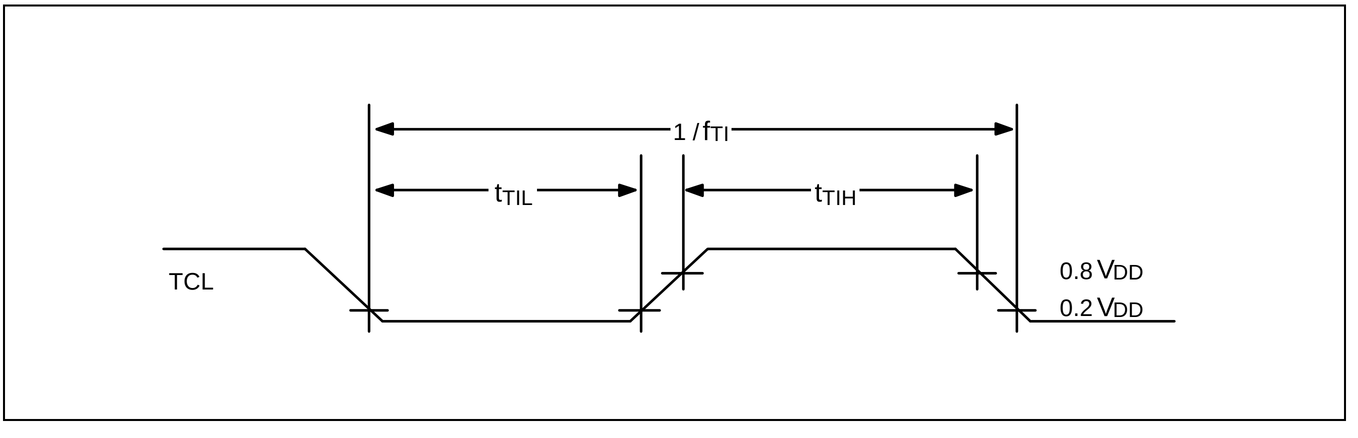


Figure 13-6. TCL Timing

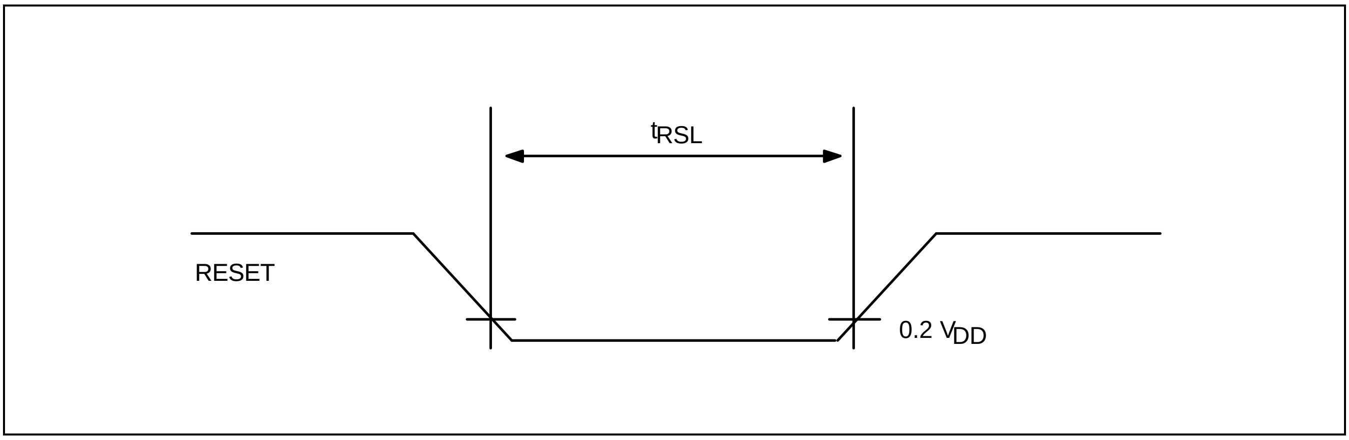


Figure 13-7. Input Timing for RESET Signal

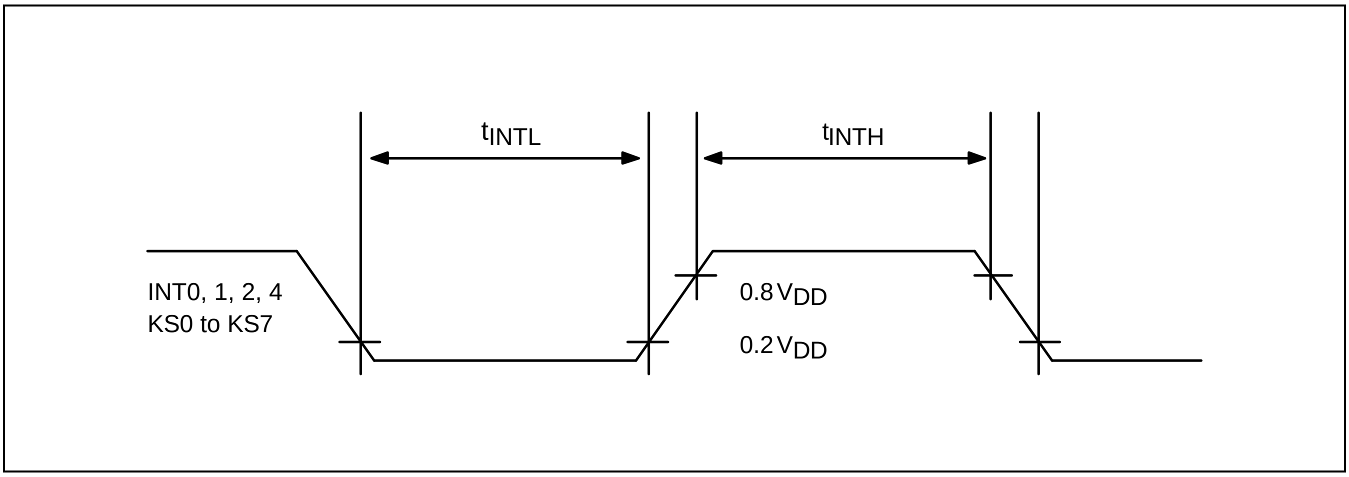


Figure 13-8. Input Timing for External Interrupts and Quasi-Interrupts

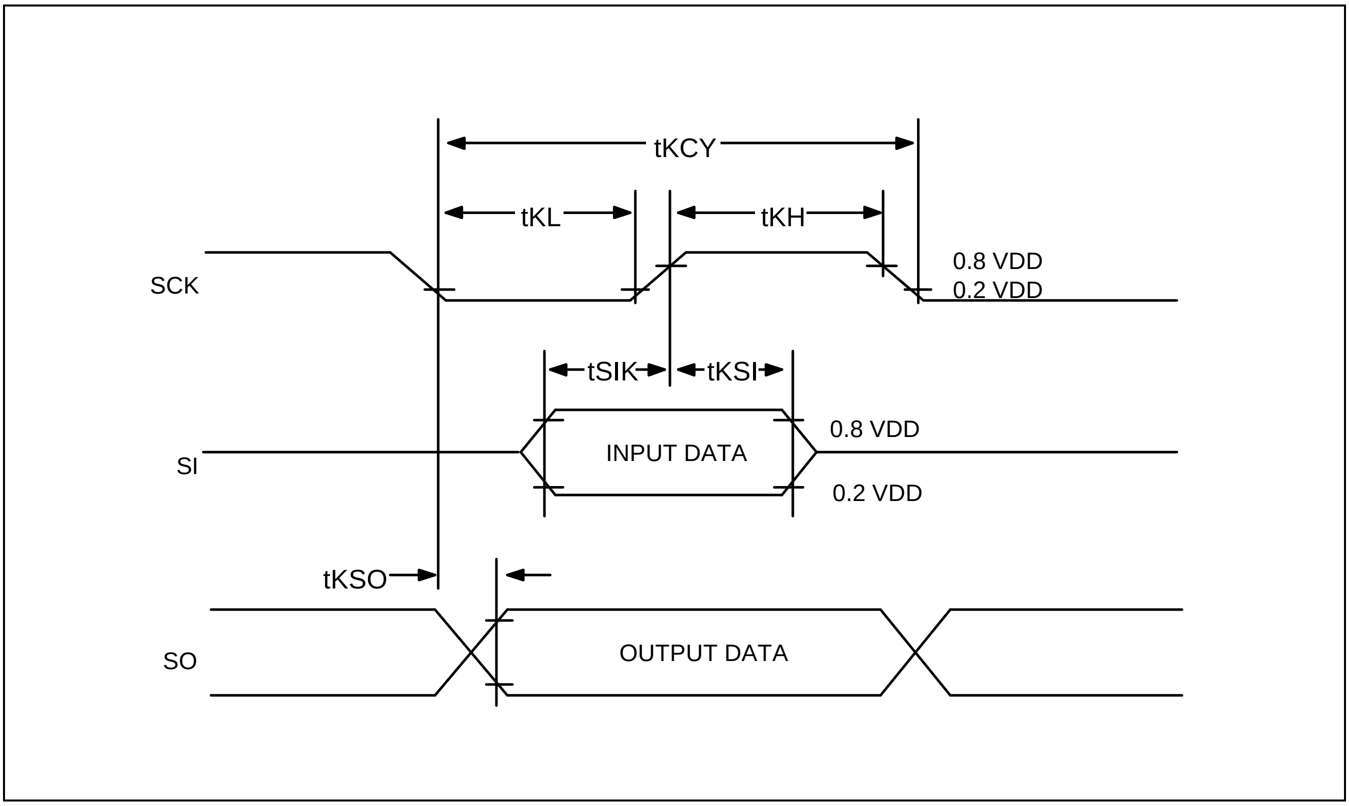


Figure 13-9. Serial Data Transfer Timing

14 MECHANICAL DATA

This section contains the following information about the device package:

— 42-SDIP-600 package dimensions in millimeters

— 44-QFP-1010B package dimensions in millimeters

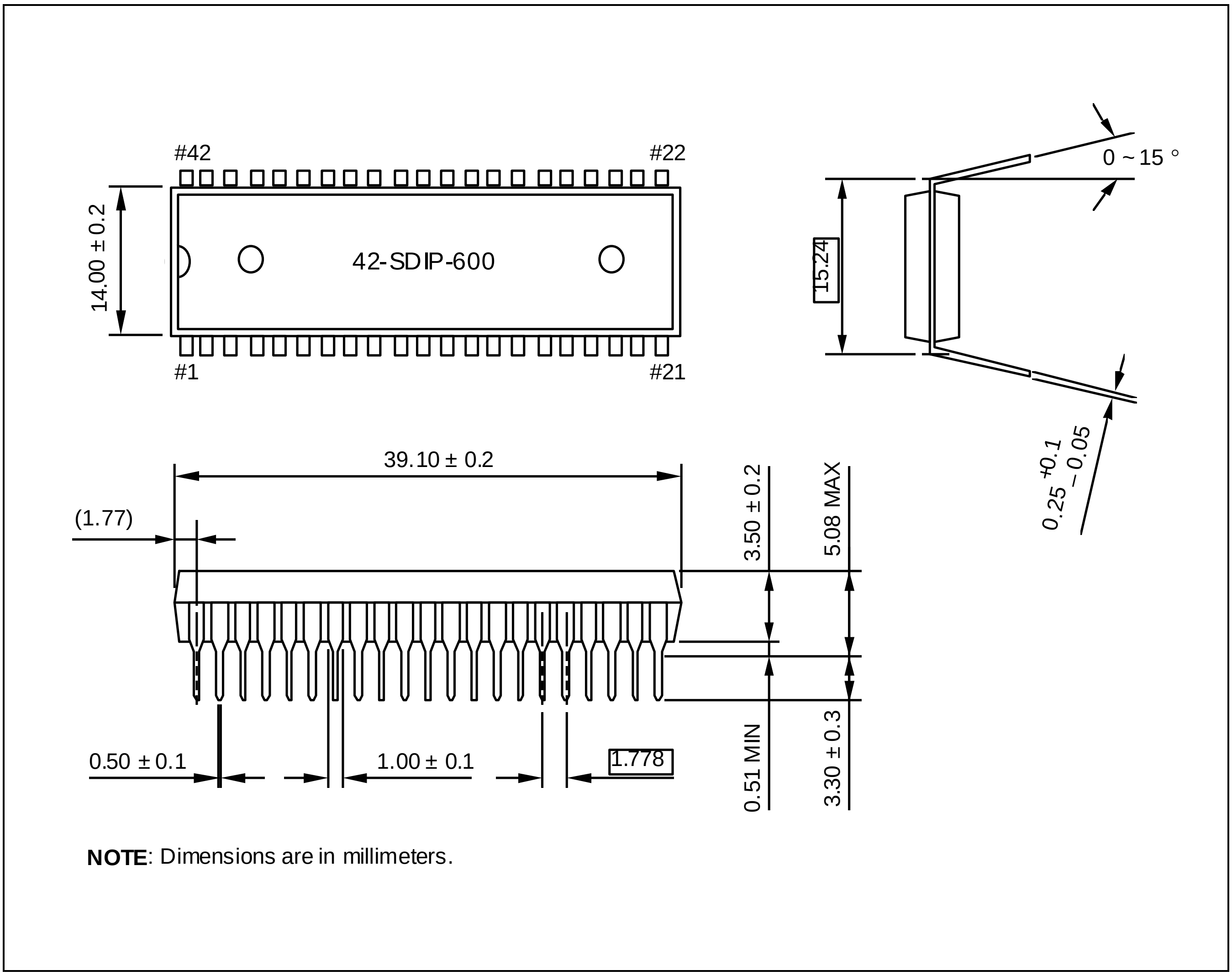
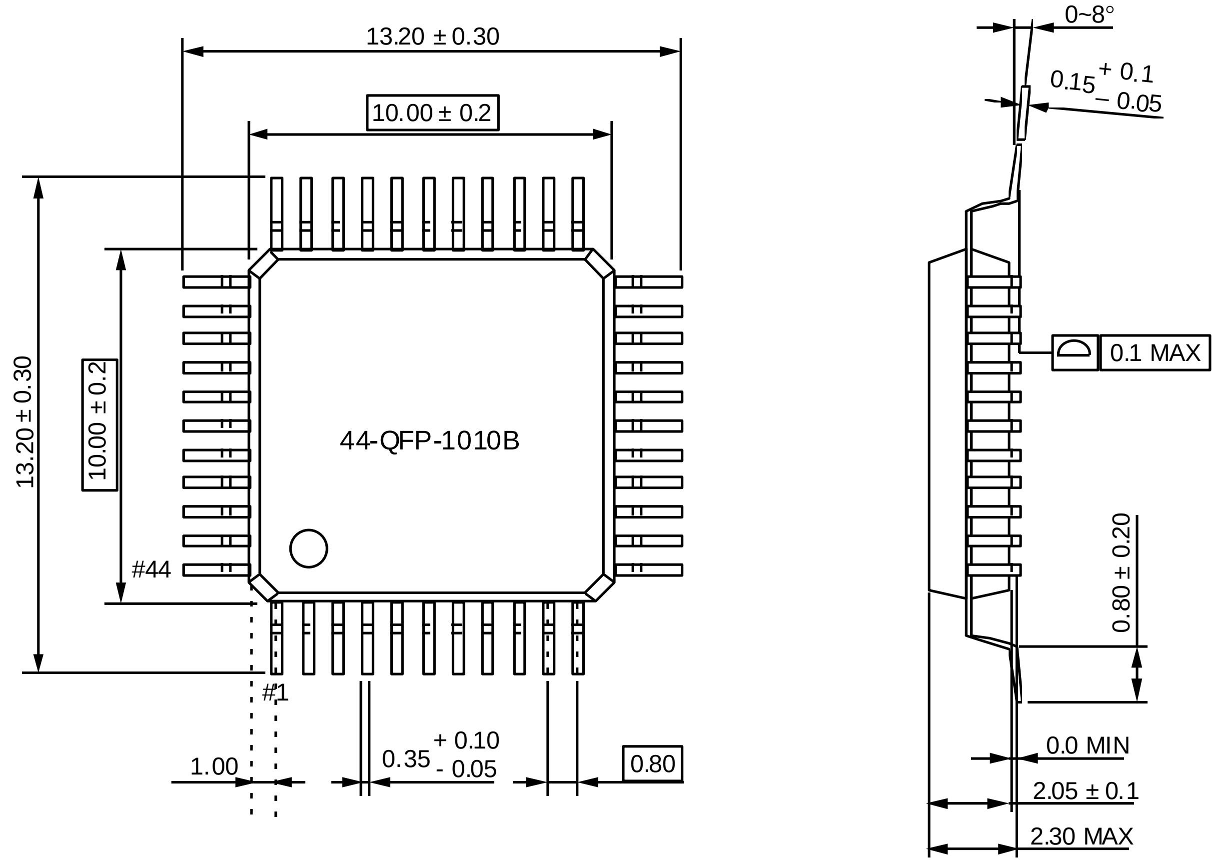


Figure 14-1. 42-SDIP-600 Package Dimensions



NOTE: Dimensions are in millimeters.

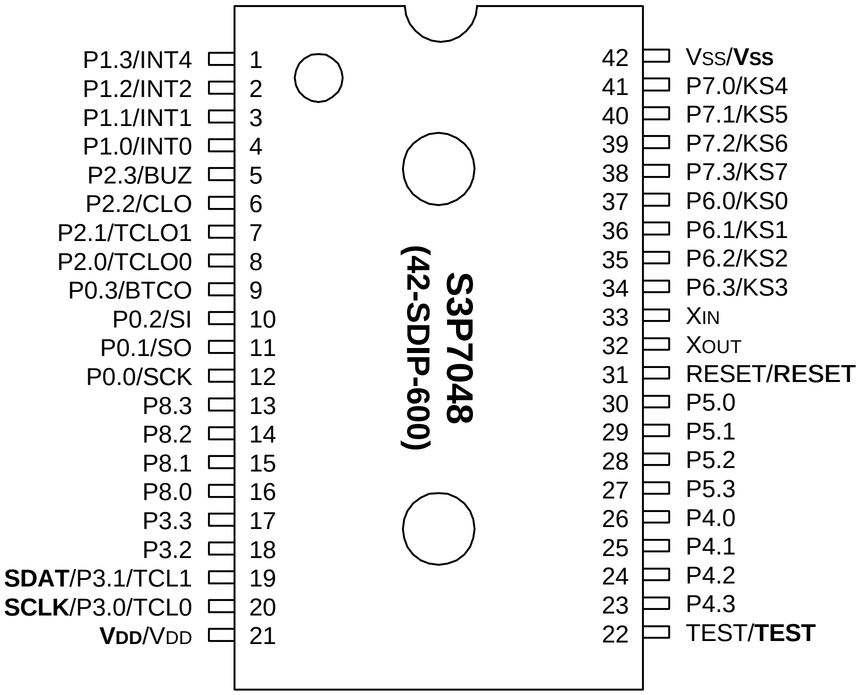
Figure 14-2. 44-QFP-1010B Package Dimensions

15 S3P7048 OTP

OVERVIEW

The S3P7048 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C7044/C7048 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P7048 is fully compatible with the S3C7044/C7048, both in function and in pin configuration. Because of its simple programming requirements, the S3P7048 is ideal for use as an evaluation chip for the S3C7044/C7048.



NOTE: The bolds indicate an OTP pin name.

Figure 15-1. S3P7048 Pin Assignments (42-SDIP Package)

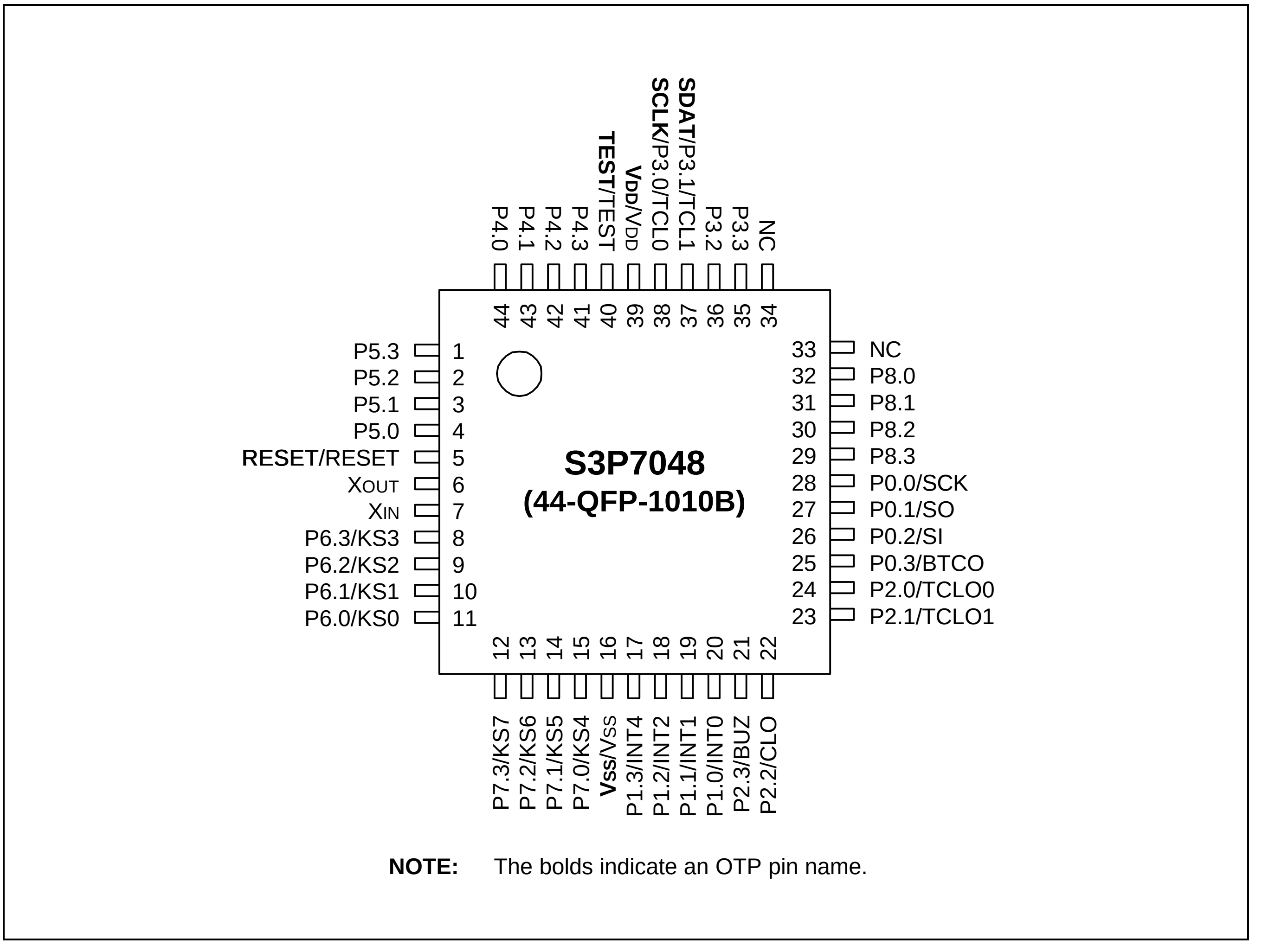


Figure 15-2. S3P7048 Pin Assignments (44-QFP Package)

Table 15-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P3.1	SDAT	19 (37)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P3.0	SCLK	20 (38)	I/O	Serial clock pin. Input only pin.
TEST	V_{PP}(TEST)	22 (40)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	31 (5)	I	Chip initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	21/42(39/16)	I	Logic power supply pin. V_{DD} should be tied to +5 V during programming.

NOTE: ( ) means the 44-QFP OTP pin number.

Table 15-2. Comparison of S3P7048 and S3C7044/C7048 Features

Characteristic	S3P7048	S3C7044/C7048
Program Memory	8 K-byte EPROM	4 K-byte mask ROM: S3C7044 8 K-byte mask ROM: S3C7048
Operating Voltage (V_{DD})	2.0 V to 5.5 V	1.8 V to 5.5V
OTP Programming Mode	V_{DD} = 5 V, V_{PP}(TEST)=12.5V	
Pin Configuration	42SDIP, 44QFP	42SDIP, 44QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP}(TEST) pin of the S3P7048, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 15-3 below.

Table 15-3. Operating Mode Selection Criteria

V_{DD}	Vpp (TEST)	REG/ MEM	Address (A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

Table 15-4. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except those specified below for V_{IH2} – V_{IH4}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 3, 6, 7, and RESET	0.8 V_{DD}			
	V_{IH3}	Ports 4 and 5 with pull-up resistors assigned	0.7 V_{DD}			
		Ports 4 and 5 are open-drain				
	V_{IH4}	X_{IN} and X_{OUT}	V_{DD} – 0.1			
Input Low Voltage	V_{IL1}	All input pins except those specified below for V_{IL2}–V_{IL3}	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 3, 6, 7, and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN} and X_{OUT}			0.1	
Output High Voltage	V_{OH}	I_{OH} = – 1 mA Ports except 1, 4, and 5	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA, Ports 4, 5 only	–	–	2	V
		V_{DD} = 2.0 to 5.5 V I_{OL} = 1.6mA			0.4	
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V I_{OL}= 4 mA All output ports except ports 4,5			2	
		V_{DD} = 2.0 to 5.5 V I_{OL} = 1.6mA			0.4	
Input High Leakage Current	I_{LIH1}	V_I = V_{DD} All input pins except those specified below for I_{LIH2}	–	–	3	μA
	I_{LIH2}	V_I = V_{DD} X_{IN} and X_{OUT}			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V All input pins except below and RESET	–	–	– 3	μA
	I_{LIL2}	V_I = 0 V X_{IN} and X_{OUT} only			– 20	

Table 15-4. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Output High Leakage Current	I_{LOH}	$V_O = V_{DD,}$ All output pins		–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V, All output pins		–	–	– 3	µA
Pull-Up Resistor	R_{L1}	V_I = 0 V; V_{DD} = 5 V Ports 0, 1 (not P1.3), 2, 3, 6, 7		25	47	100	kΩ
		V_{DD} = 3 V		50	95	200	
	R_{L2}	$V_O = V_{DD}$ – 2V; V_{DD} = 5V Ports 4 and 5 only		15	47	70	
		V_{DD} = 3 V		10	45	60	
	R_{L3}	V_{DD} = 5 V; V_I = 0V; RESET		100	220	400	
		V_{DD} = 3 V		200	450	800	
Pull-Down Resistor	R_{L4}	V_{DD} = 5 V; $V_I = V_{DD}$; Port 8		25	47	100	kΩ
		V_{DD} = 3 V		50	95	200	
Supply Current (1)	I_{DD1}	Run mode; V_{DD} = 5 V ± 10%	6.0 MHz	–	3.9	8.0	mA
		Crystal oscillator; C1 = C2 = 22 pF	4.19 MHz		2.9	5.5	
		V_{DD} = 3 V ± 10%	6.0 MHz		1.8	4.0	
			4.19 MHz		1.3	3.0	
	I_{DD2}	Run mode; V_{DD} = 5 V ± 10%	6.0 MHz	–	1.3	2.5	mA
		crystal oscillator, C1 = C2 = 22 pF	4.19 MHz		1.2	1.8	
		V_{DD} = 3 V ± 10%	6.0 MHz		0.5	1.5	
			4.19 MHz		0.44	1.0	
	I_{DD3}	Stop mode; V_{DD} = 5 V ± 10%		–	0.2	3	µA
		Stop mode; V_{DD} = 3 V ± 10%			0.1	2	

NOTES

1. D.C. electrical values for Supply Current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up resistors.
2. The supply current assumes a CPU clock of fx/4.

Table 15-5. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 2.0 V to 5.5 V	0.95			
TCL0, TCL1 Input Frequency	f_{TI0}, f_{TI1}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 2.0 V to 5.5V			1	
TCL0, TCL1 Input High, Low Width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 2.0 V to 5.5 V	1.8			
SCK Cycle Time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V External SCK source	800	–	–	µs
		Internal SCK source	670			
		V_{DD} = 2.0 V to 5.5 V External SCK source	3200			
		Internal SCK source	3800			
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 2.7 V to 5.5 V External SCK source	335	–	–	µs
		Internal SCK source	t_{KCY}/ 2 – 50			
		V_{DD} = 2.0 V to 5.5 V External SCK source	1600			
		Internal SCK source	t_{KCY}/ 2 – 150			

Table 15-5. A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SI Setup Time to SCK High	t_{SIK}	V_{DD} = 2.7 V to 5.5 V External SCK source	100	–	–	ns
		Internal SCK source	150			
		V_{DD} = 2.0 V to 5.5 V External SCK source	150			
		Internal SCK source	500			
SI Hold Time to SCK High	t_{KSI}	V_{DD} = 2.7 V to 5.5 V External SCK source	400	–	–	ns
		Internal SCK source	400			
		V_{DD} = 2.0 V to 5.5 V External SCK source	600			
		Internal SCK source	500			
Output Delay for SCK to SO	t_{KSO} (1)	V_{DD} = 2.7 V to 5.5 V External SCK source	–	–	300	ns
		Internal SCK source			250	
		V_{DD} = 2.0 V to 5.5 V External SCK source			1000	
		Internal SCK source			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0	(2)	–	–	µs
		INT1, INT2, INT4, KS0 - KS7	10			
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTES
1. R (1KΩ) and C (100pF) are the load resistance and load capacitance of the SO output line.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128/fx as assigned by the IMOD0 register setting.

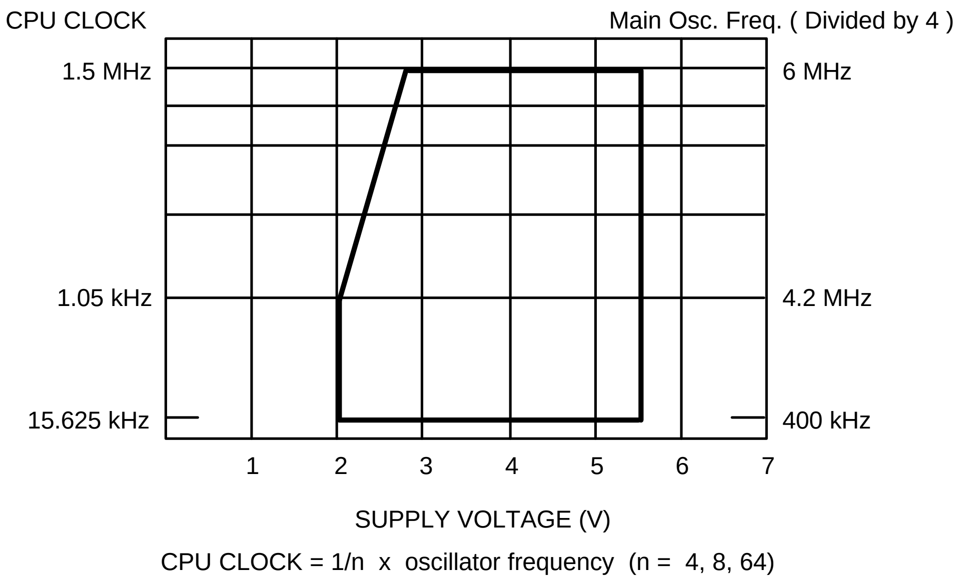


Figure 15-3. Standard Operating Voltage Range

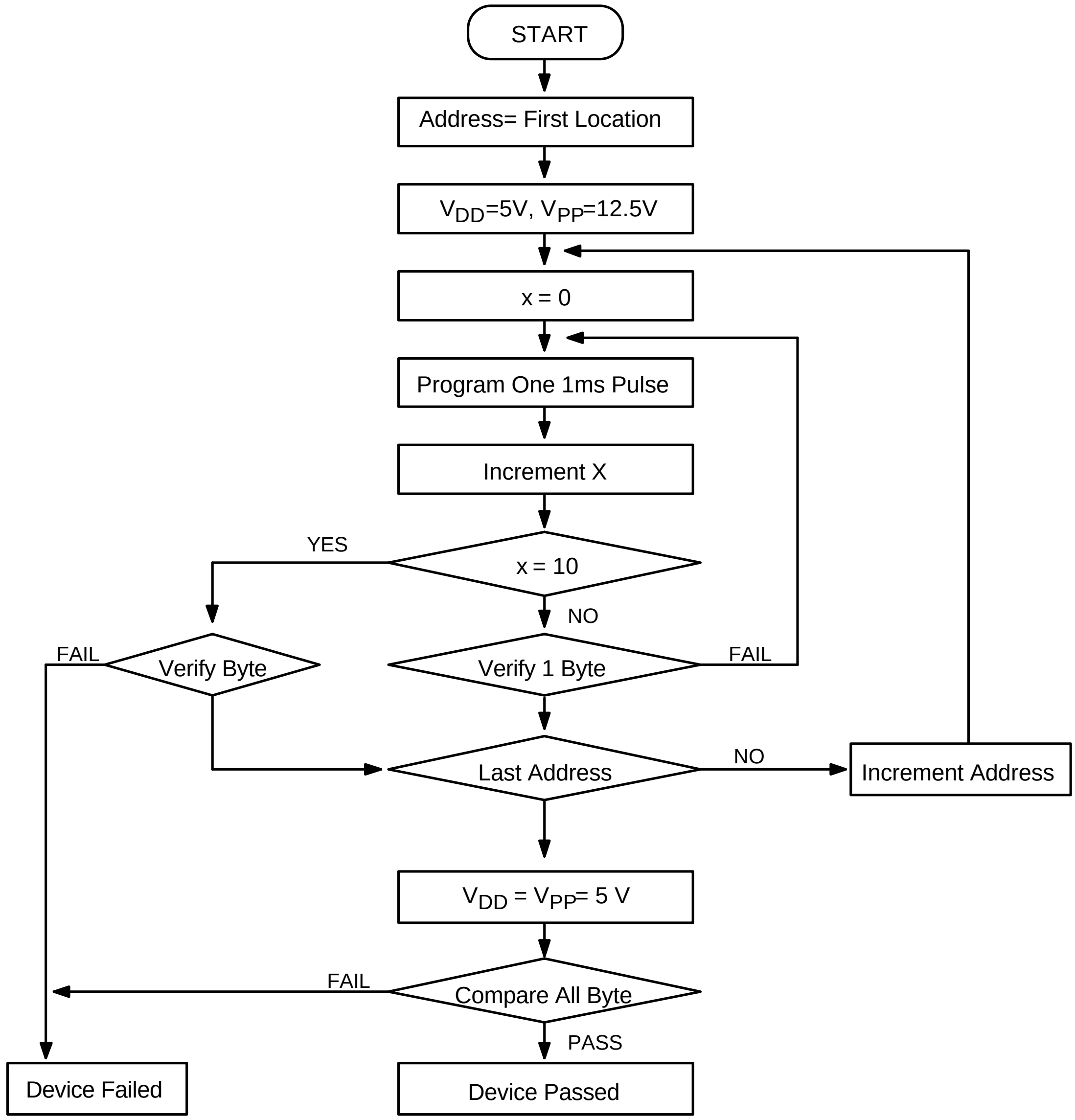


Figure 15-4. OTP Programming Algorithm